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L1: Entry 15 of 21 File: USPT Jun 8, 1999

DOCUMENT-IDENTIFIER: US 5911149 A
TITLE: Apparatus and method for implementing a programmable shared memory with dual bus architecture

Abstract Paragraph Left (1):
A computer system having a processor and at least one peripheral has a programmable shared memory system and method that selectively dedicates a first potion of memory to use by the processor and allocates a second portion of memory to shared use by the processor and any peripherals in the system. The programmable memory architecture is implemented using a dual bus architecture having a first-bus connected to the processor and a second bus coupled to the processor by a system controller and to the peripherals by a peripheral controller. The programmable memory architecture additionally has a configuration controller coupled to each configurable memory bank in the system. Each configuration controller is additionally coupled to both the first and second buses. Under programmed control, the each configuration controller couples the associated memory to either the first or second bus, responsive to configuration information stored in the system controller. Memory coupled to the first bus operates as dedicated processor memory and memory coupled to the second bus operates as shared memory, accessible by the processor and any peripherals in the system.

Brief Summary Paragraph Right (7):
In accordance with the present invention, there is provided a programmable shared memory system and method that improves memory utilization, decreases overall system memory requirements and costs and does not degrade system performance. The programmable shared memory system and method selectively dedicates a first portion of memory to use by a processor and allocates a second portion of memory to shared use by the processor and any peripherals in the system. The programmable memory architecture is implemented using a dual bus architecture and a plurality of configurable memory banks. The dual bus architecture has a first bus connected to the processor and a second bus coupled to the peripherals by peripheral controllers and also coupled to the processor by a system controller.

Brief Summary Paragraph Right (8):
Also in accordance with the invention, the programmable memory architecture has a configuration controller coupled to each configurable memory bank. Each configuration controller is additionally coupled to both the first and second buses. Under programmed control, each configuration controller couples the associated memory to either the first or second bus, responsive to configuration information stored in the system controller. Memory coupled to the first bus (the processor bus) operates as dedicated processor memory and memory coupled to the second bus (the shared memory bus) operates as shared memory, accessible by the processor and any peripherals in the system.

L1: Entry 18 of 21 File: USPT Sep 1, 1998

DOCUMENT-IDENTIFIER: US 5801547 A
TITLE: Embedded memory for field programmable gate array

Brief Summary Paragraph Right (16):
The present invention provides a programmable logic device having a configuration memory, which is partitioned so that it includes at least one subarray available through the user configurable logic to be used as memory in the user's design. According to the present invention, the configuration memory is accessible using global configuration memory access logic normally used for loading configuration programs into the programmable logic device. In addition, subarrays of the configuration memory have independent access logic coupled with them, and coupled to the user logic array so that they may be used independently as user memory.

Brief Summary Paragraph Right (18):
The present invention can also be characterized as a programmable logic device having an SRAM based configuration memory, and global memory access logic coupled with the configuration memory. The global memory access logic is utilized for reading and writing programs for configuration of the programmable logic device. One of the configuration options available according to the present invention is to segment the configuration memory, such that subarrays are utilized as user memory. Thus, the programmable logic device of the present invention includes a plurality of subarrays of SRAM memory elements within the configuration memory. A plurality of subarray decoders with corresponding configurable interconnect circuits coupled to the configurable logic array are associated with corresponding subarrays of the configuration memory. Also a plurality of subarray I/O path circuits are associated with corresponding subarrays in the configuration memory. Configurable interconnect circuits are coupled with corresponding subarray decoders. These interconnect circuits include a programmable switch including inputs connected to the configurable logic array, and including both outputs connected to the configurable logic array and outputs connected to the subarray decoder for the corresponding subarray. Also, configurable interconnect circuits for corresponding subarray I/O paths are included. These configurable interconnect circuits include a programmable switch having inputs connected to the configurable logic array, and inputs connected to the subarray I/O path for the corresponding subarray. The outputs of a programmable switch associated with a subarray I/O path circuit include outputs connected to configurable logic array, and outputs connected to the subarray I/O path circuit for the corresponding subarray. Using these configurable interconnect circuits, a subarray of the configuration memory can be connected for use as user memory, used as normal configuration memory specifying the logic functions of the corresponding subarray of the configurable logic array or, with careful layout, used in part) for memory and in part for logic configuration. To use a subarray for both logic configuration and memory, the design must ensure that the subset of the subarray accessed for memory locations does not overlap the subset used for configuring routing and logic resources.

Partition

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L2: Entry 5 of 7 File: USPT Sep 1, 1998

DOCUMENT-IDENTIFIER: US 5801547 A
TITLE: Embedded memory for field programmable gate array

Abstract Paragraph Left (1):
A programmable logic device has a configuration memory which is partitioned so that it includes at least one subarray available through the programmable interconnect of the user configurable logic to be used as user memory. Subarrays of the configuration memory have independent access logic coupled with them, and coupled to the user logic array so that they may be used independently as user memories. Subarray memory access logic is provided for each subarray of memory elements, and connected to the logic cell array, and optionally to the plurality of input/output cells on the device, including a subarray decoder used for selecting addressed memory elements in the corresponding subarray in response to address signals and control signals supplied across the interconnect structures of the logic cell array, and a subarray I/O path used to provide input and output data signals between the interconnect structures of the logic cell array and addressed memory elements in the subarray. Thus, each subarray of memory elements, its corresponding subarray decoder and subarray I/O path, are independently configurable in the programmable logic device for use as user memory.

Brief Summary Paragraph Right (16):
The present invention provides a programmable logic device having a configuration memory, which is partitioned so that it includes at least one subarray available through the user configurable logic to be used as memory in the user's design. According to the present invention, the configuration memory is accessible using global configuration memory access logic normally used for loading configuration programs into the programmable logic device. In addition, subarrays of the configuration memory have independent access logic coupled with them, and coupled to the user logic array so that they may be used independently as user memory.

Brief Summary Paragraph Right (18):
The present invention can also be characterized as a programmable logic device having an SRAM based configuration memory, and global memory access logic coupled with the configuration memory. The global memory access logic is utilized for reading and writing programs for configuration of the programmable logic device. One of the configuration options available according to the present invention is to segment the configuration memory, such that subarrays are utilized as user memory. Thus, the programmable logic device of the present invention includes a plurality of subarrays of SRAM memory elements within the configuration memory. A plurality of subarray decoders with corresponding configurable interconnect circuits coupled to the configurable logic array are associated with corresponding subarrays of the configuration memory. Also a plurality of subarray I/O path circuits are associated with corresponding subarrays in the configuration memory. Configurable interconnect circuits are coupled with corresponding subarray decoders. These interconnect circuits include a programmable switch including inputs connected to the configurable logic array, and including both outputs connected to the configurable logic array and outputs connected to the subarray decoder for the corresponding subarray. Also, configurable interconnect circuits for corresponding subarray I/O paths are included. These configurable interconnect circuits include a programmable switch having inputs connected to the configurable logic array, and inputs connected to the subarray I/O path for the corresponding subarray. The outputs of a programmable switch associated with a subarray I/O path circuit include outputs connected to configurable logic array, and outputs connected to the subarray I/O path circuit for the corresponding subarray. Using these configurable interconnect circuits, a subarray of the configuration memory can be connected for use as user

memory, used as normal configuration memory specifying the logic functions of the corresponding subarray of the configurable logic array or, with careful layout, used in part) for memory and in part for logic configuration. To use a subarray for both logic configuration and memory, the design must ensure that the subset of the subarray accessed for memory locations does not overlap the subset used for configuring routing and logic resources.

Brief Summary Paragraph Right (20):
The present invention is particularly suited to FPGA type programmable logic devices with SRAM based configuration memory. The partitioning of the configuration memory into subarrays, and the providing of independent memory access logic for each subarray, provides a user the ability to set up memories in the programmable logic device near the logic resources which require the memory. Also, use of the interconnect structure in the logic cell array for routing data and addresses to the memory subarrays allows flexibility in the placement and routing of logic on the device, because signals can "fly over" the memory subarray used as user memory to allow flexible interconnection of the surrounding logic. This way, the subarrays can be positioned throughout the device as suits the needs of a particular implementation.

Drawing Description Paragraph Right (3):
FIG. 3 illustrates the layout of one example FPGA architecture in which the configuration memory is partitioned into a plurality of subarrays according to the present invention.

Detailed Description Paragraph Right (5):
FIG. 3 shows the layout of an FPGA device including resources to partition the configuration memory into a plurality of subarrays that are independently accessible. FIG. 3 shows a subset of a larger device, including configuration memory subarrays for corresponding 16.times.16 logic cell blocks on the device. Thus, a first subarray 100 provides a configuration memory for a 16.times.16 logic cell block. Sixteen logic cells (e.g. cell 101) form a 4.times.4 unit 109 of cells. Twelve other 4.times.4 units (e.g. 4.times.4 units 110, 111, 112), are illustrated within the subarray 100. Each cell within a 4.times.4 block is able to drive output signals to, and receive input signals from, its nearest neighbors to the north, south, east and west in the layout. In addition, cells at the 4.times.4 block boundaries are able to drive their outputs onto length-four flyovers in the programmable interconnect. Special switch units are provided around each 4.times.4 block boundary to facilitate these connections. These switches are not shown in this example for clarity. In addition to routing signals to their nearest neighbors, each cell includes an output that is routed to other destinations, such as to switches at the boundaries of the 4.times.4 unit in which the cell is found. The configuration memory controls the switches on the boundaries for the purpose of routing signals among the interconnect structure and the user logic cells.

Detailed Description Paragraph Right (28):
A concern in the design of the embedded memory of the present invention, is that the number of wires required by the embedded addresses, data, and control to the subarray match up well with a number neighboring of user routing resources available in the array. Thus, availability of resources must be taken into account to make sure that the address and data busses can be connected using the interconnect structure of the device, and that routing congestion is avoided within the user design when a subarray of the configuration memory is partitioned for this purpose. Another concern in the design is that the layout of the memory access logic data input/output logic and of the address and control logic, associated with the subarray should not unduly increase the pitch of a set of programmable cells associated with the subarray, and thereby create unacceptable area overhead in the layout of the chip. The size of the data I/O logic 121 is influenced to a large extent by the width of the external data bus it provides, memory with an eight bit data bus having smaller word logic than one with a 32 bit bus.

Detailed Description Paragraph Right (31):
Accordingly, the present invention provides partitioning of a single large configuration memory on an FPGA into several smaller memory units. In this case, a large memory for programming an array of user logic cells, where each logic cell has

a program memory area, for example 8 bits high by 3 words wide, is broken down into a 4.times.4 array of smaller 16.times.16 unit subarrays, each subarray corresponding to configuration memory for a 16.times.16 array of logic cells. Partitioning the memory in this way increases area of the layout of the chip, because multiple sets of memory access logic are required, one for each subarray. Also there is area overhead in routing address and data signals to the individual subarrays. However, smaller memories are likely to be faster and more flexible than a larger memory, and may be operated independently. This greatly increases the flexibility of the FPGA device for implementing small areas of user memory adjacent to the logic which uses the memory.